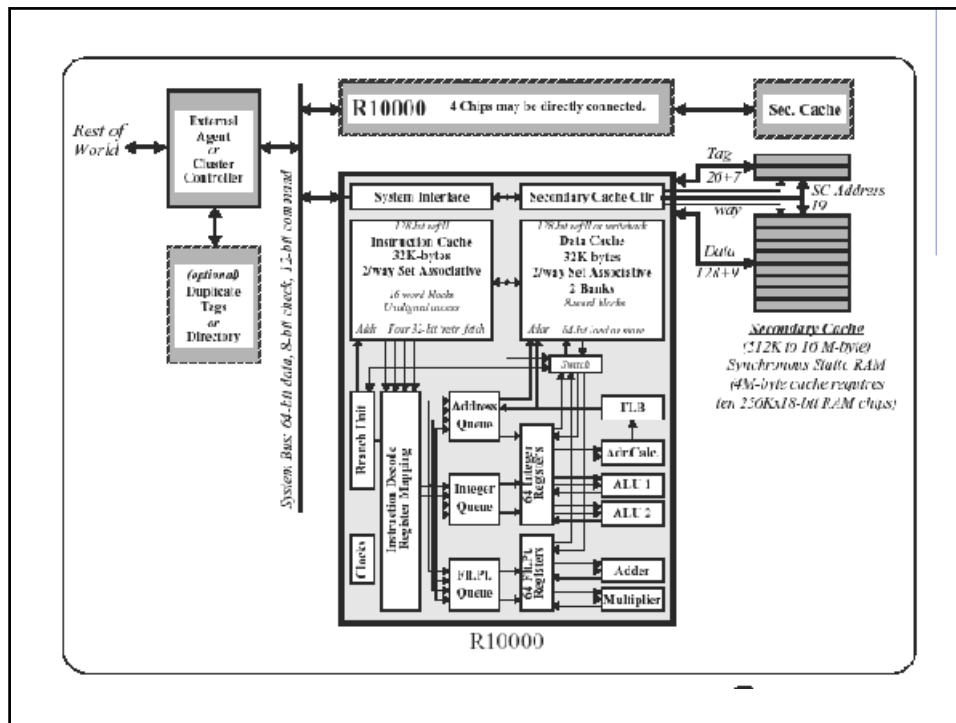


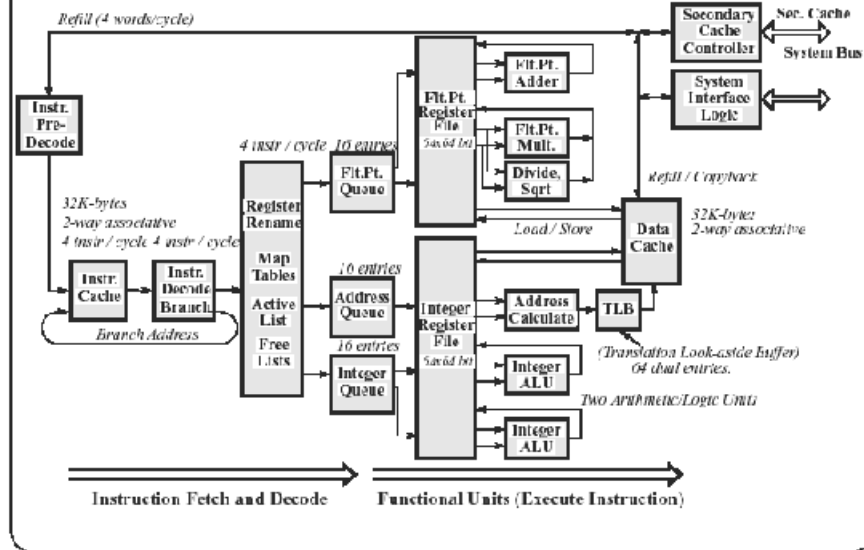
Microarquitecturas de Alto Desempenho

MIPS R10000

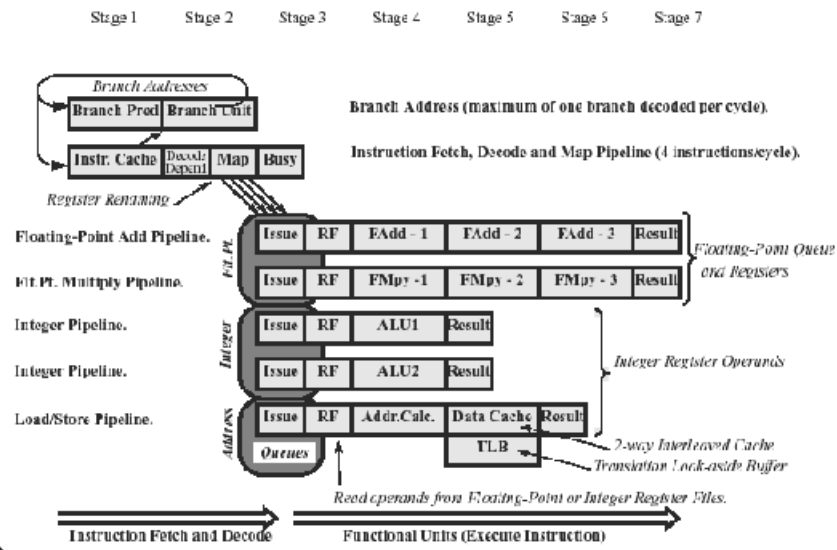
Gabriel P. Silva



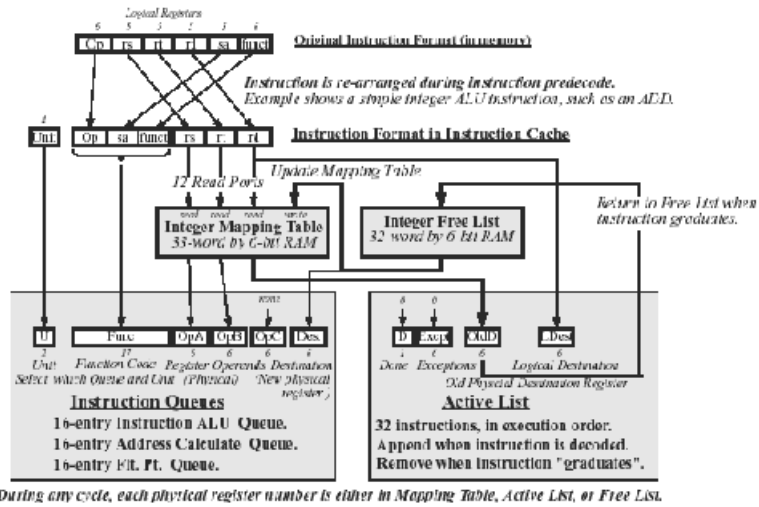
R10000 - Block Diagram



R10000 - Pipelines



Register Renaming



Control Paths

Fetch and Decode

4 Instructions per cycle

op rs rt rd sh funct

Logical registers

5 bits

6 bits

Ordered list of instructions.

List of unused registers.

Register Renaming

6-bit Control Logic

3 Instr Queues

Dynamic Instruction Issue

Physical registers

16 entries

64-bit

64 bits

No reservation stations or re-ordering buffers.

Operands are bypassed or read directly from Register File.

Results are written directly back into Register File.

Queue

Register File

Execution Unit

Latency

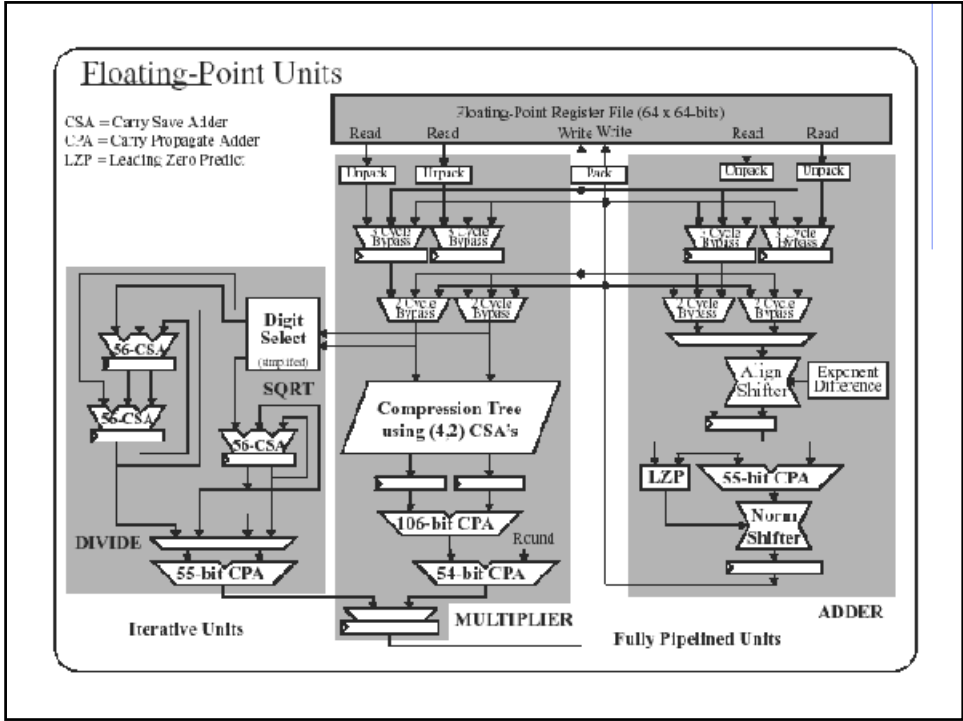
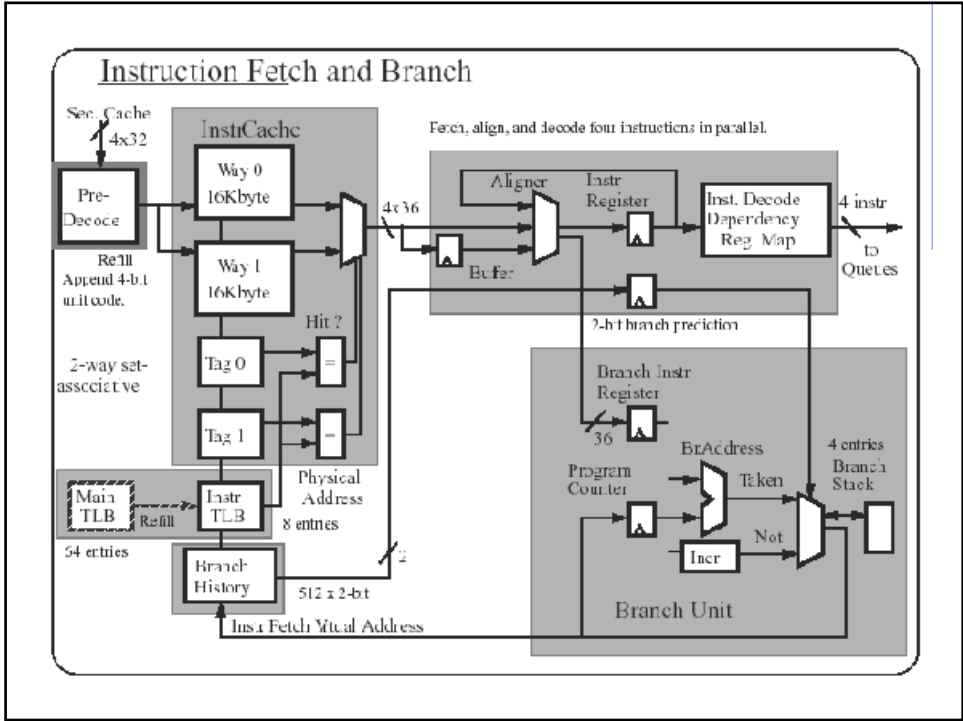
Integer Integer ALU 1 1

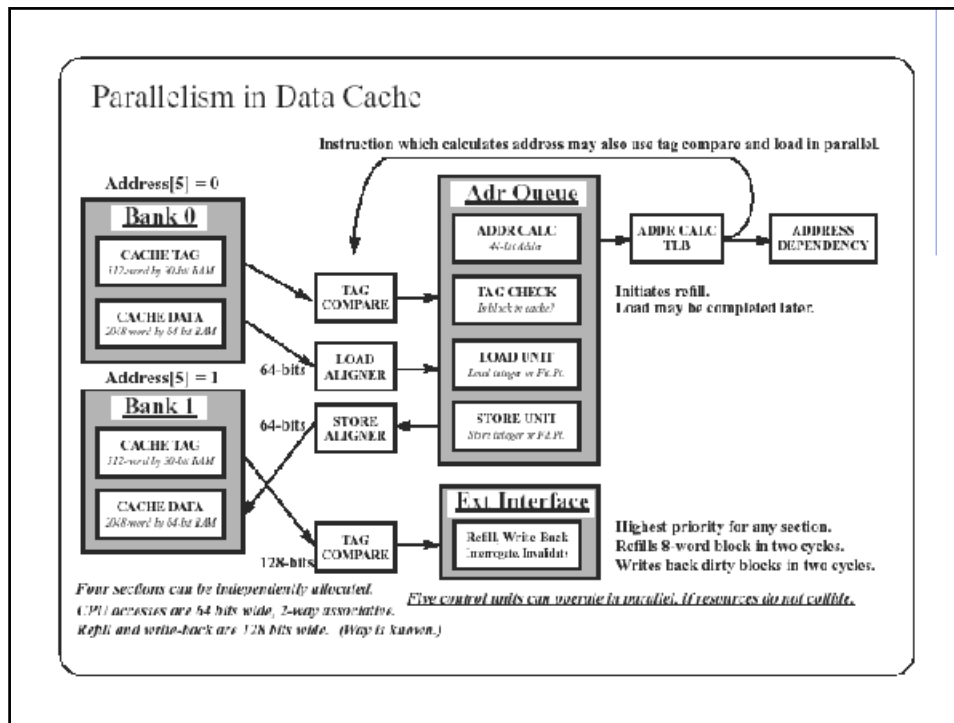
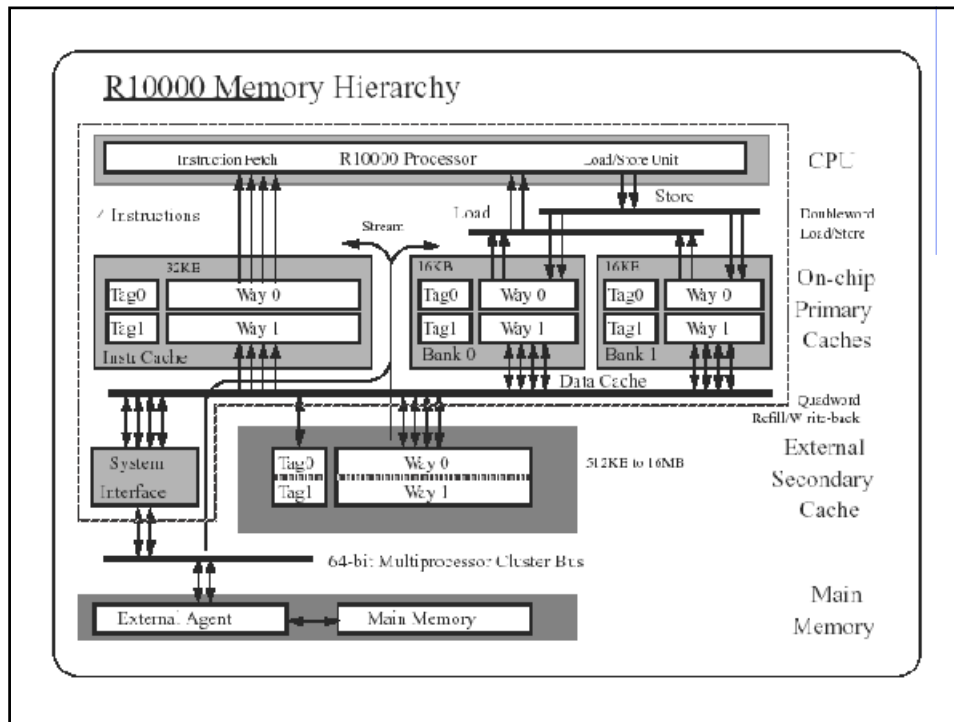
Integer Integer ALU 2 1

Address Integer Address Calculation 2

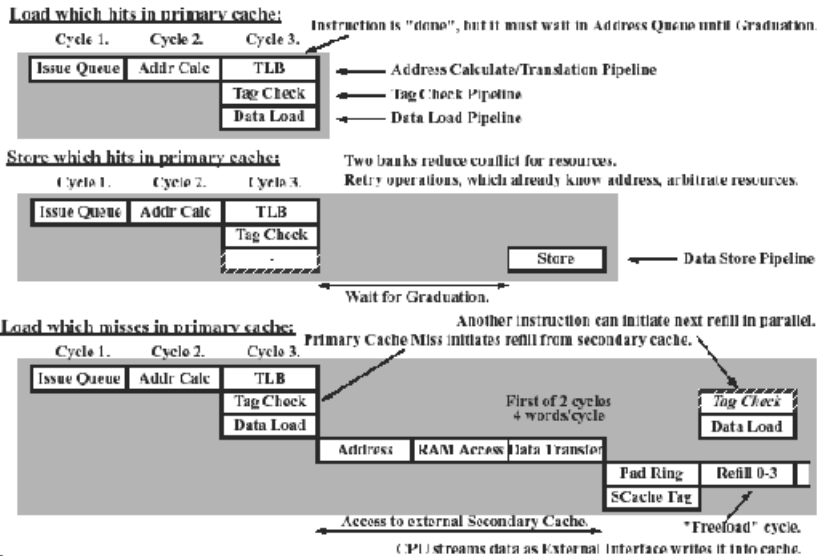
Flt.Pt. Flt.Pt. Flt.Pt. Adder 2

Flt.Pt. Flt.Pt. Flt.Pt. Multiplier 2

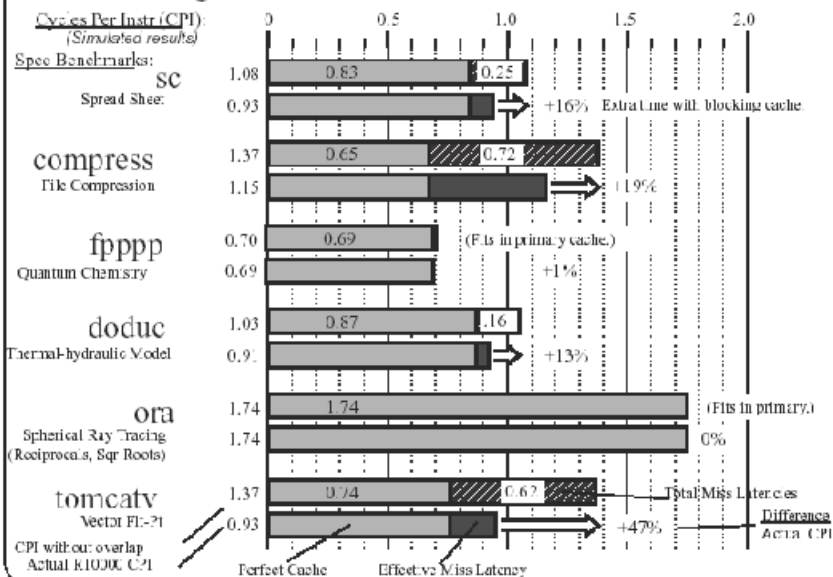




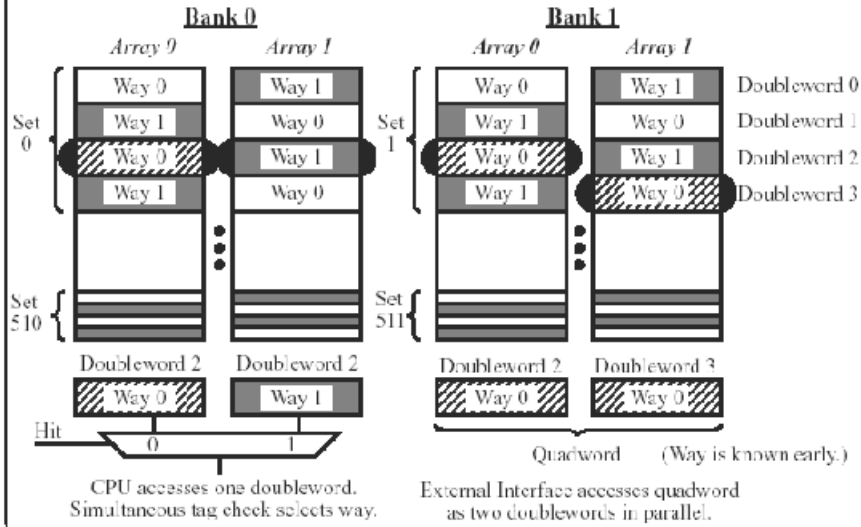
Data Cache Pipelines



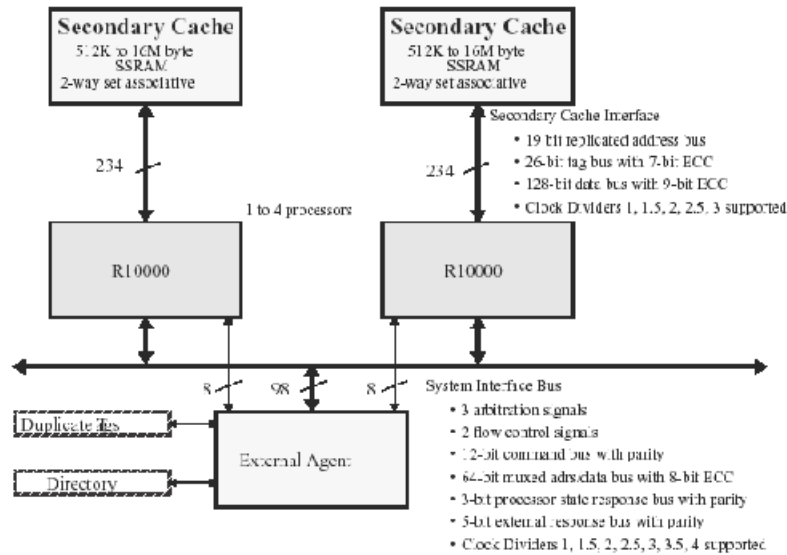
Non-blocking Cache

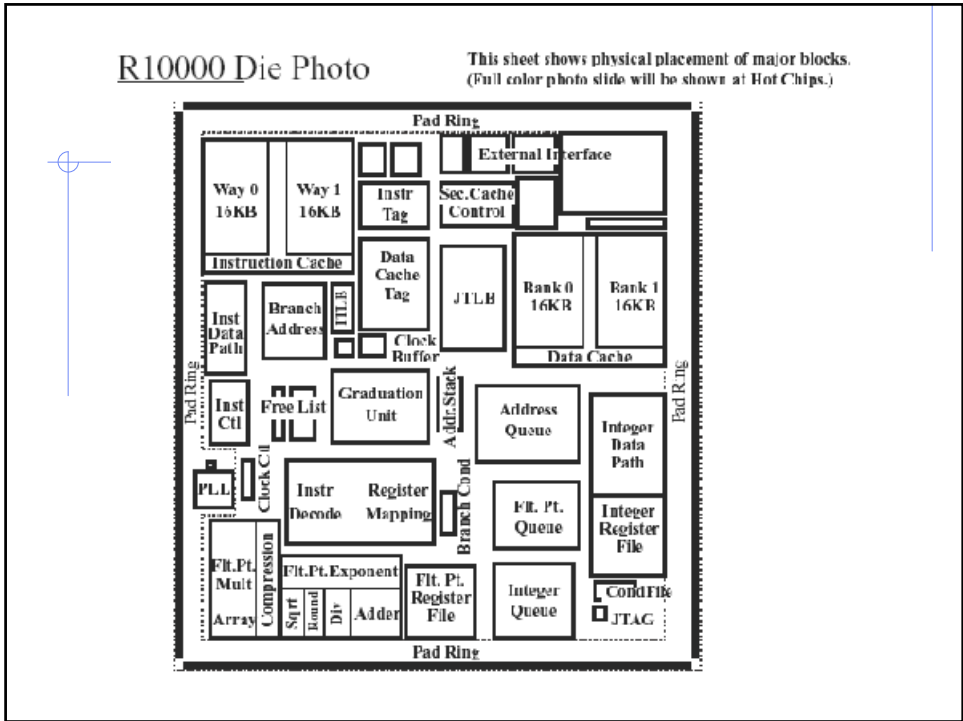
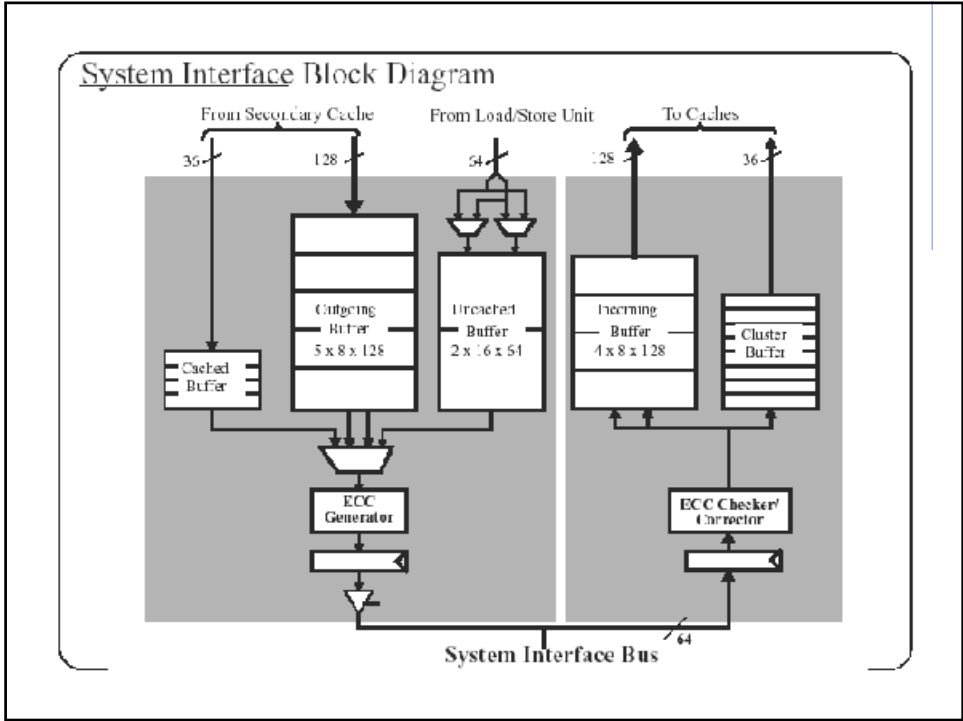


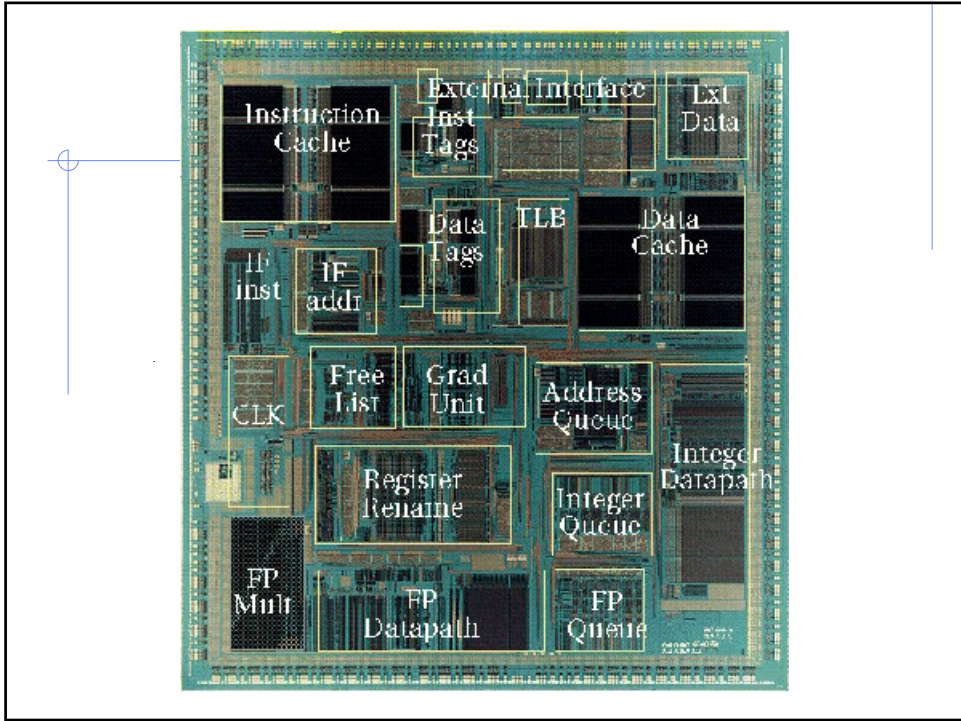
Data Cache Interleaving



System Configurations







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