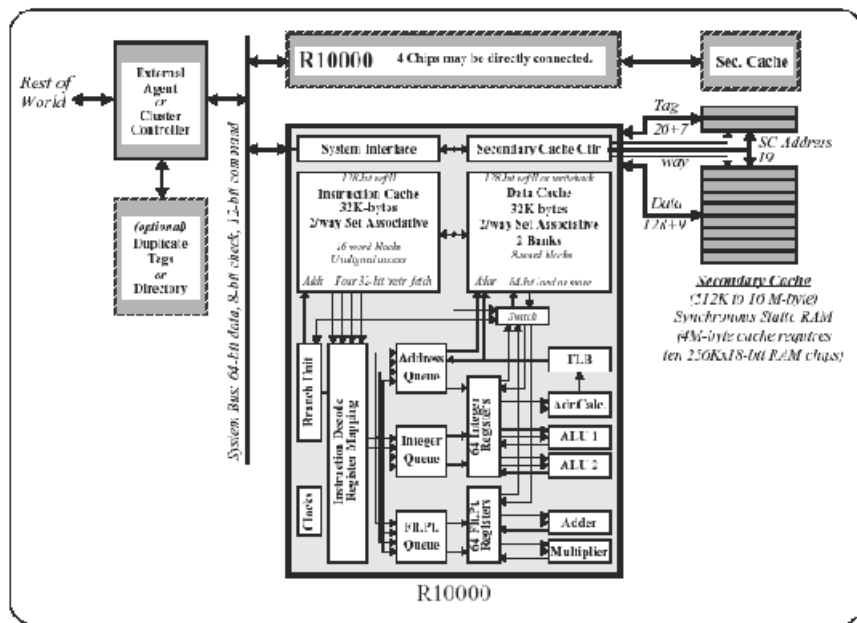


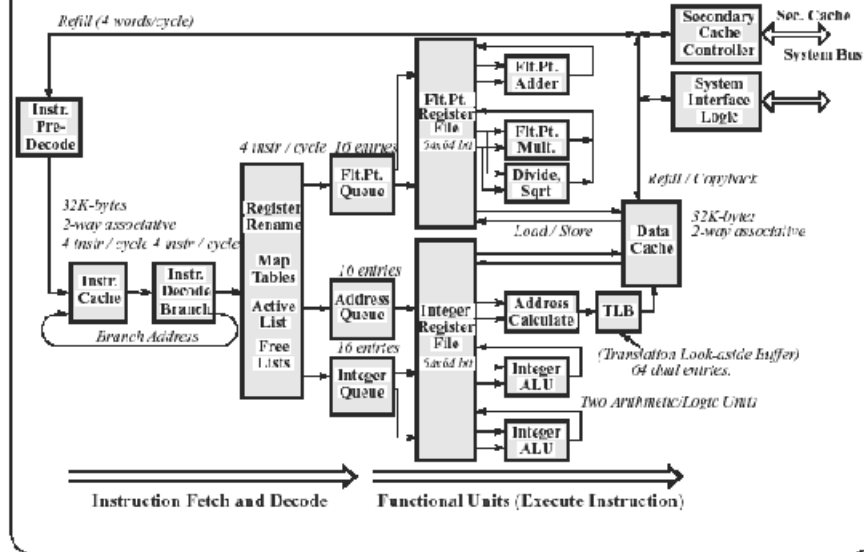
Microarquitecturas de Alto Desempenho

MIPS R10000

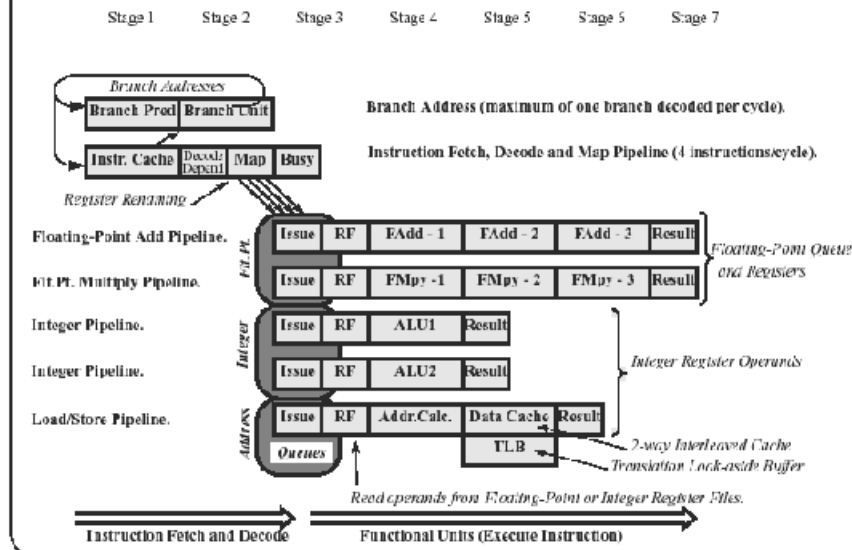
Gabriel P. Silva



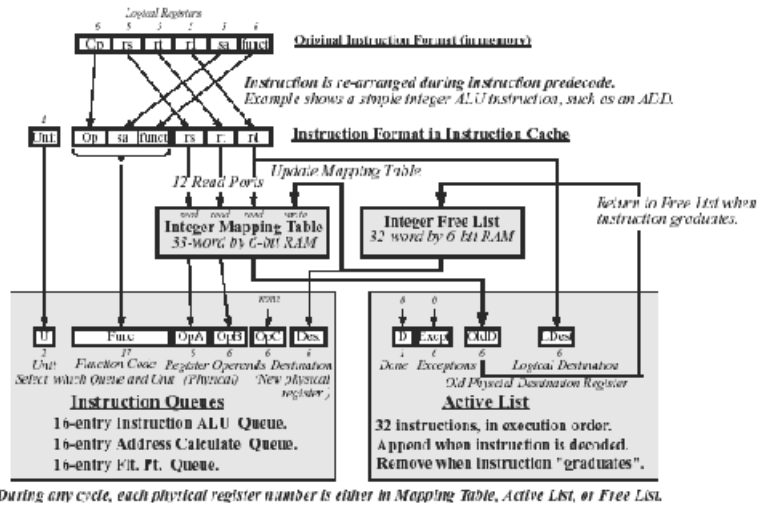
R10000 - Block Diagram



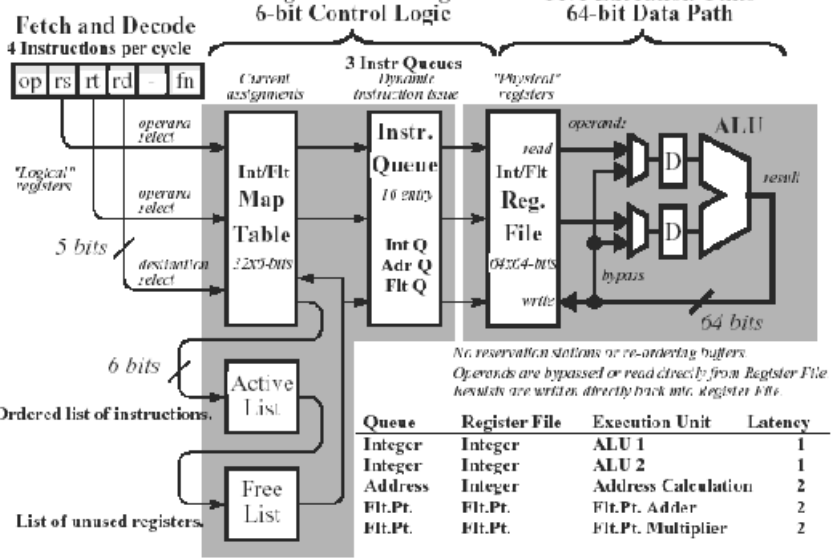
R10000 - Pipelines

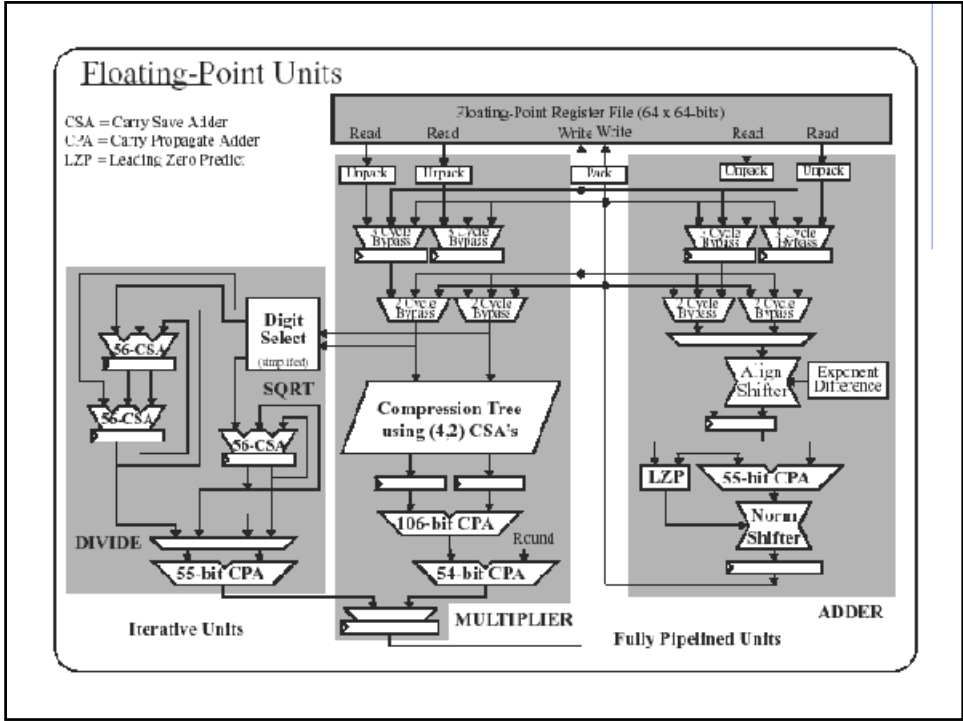
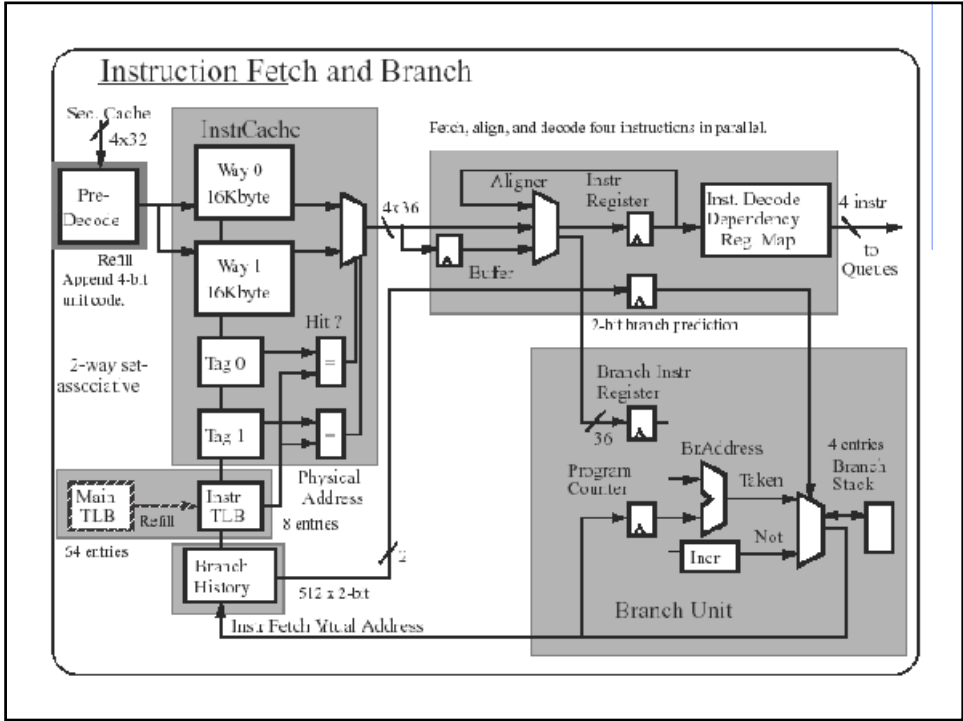


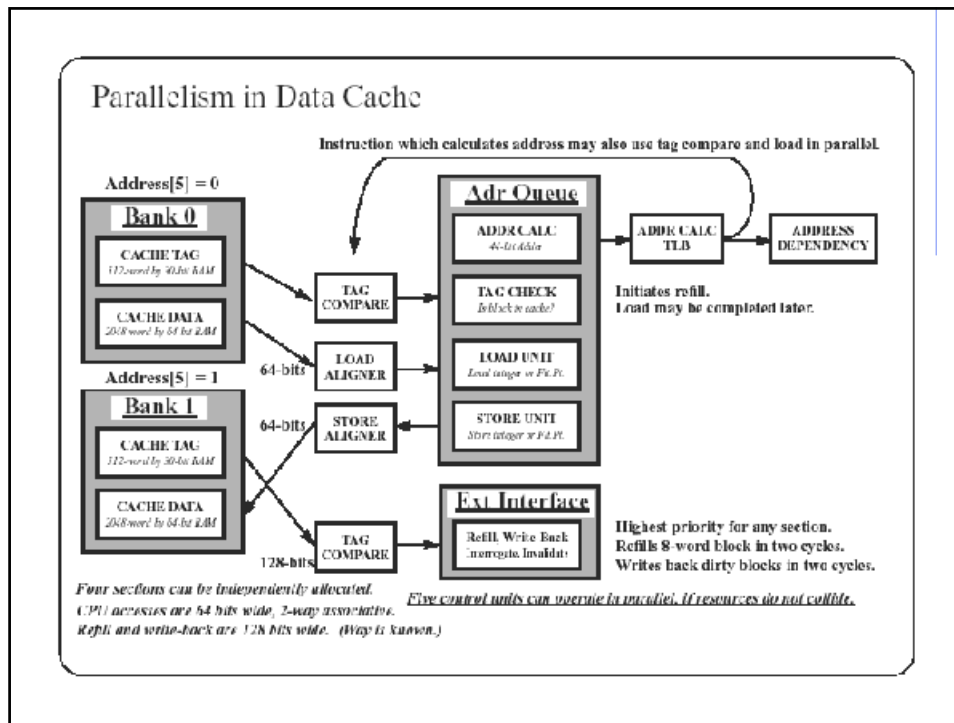
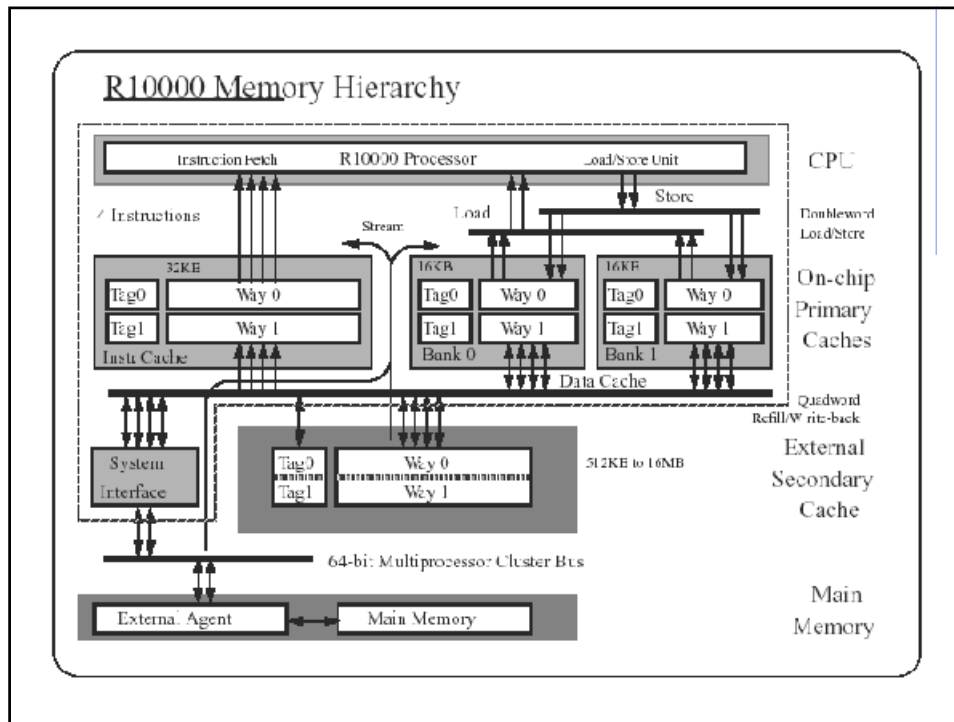
Register Renaming



Control Paths

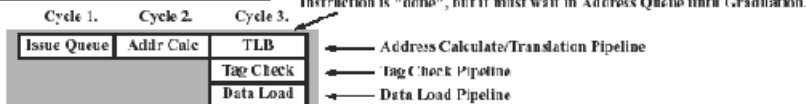




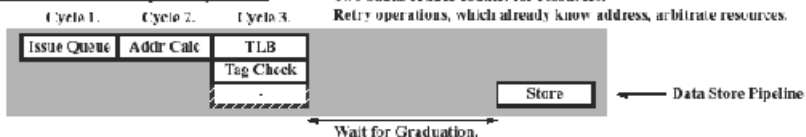


Data Cache Pipelines

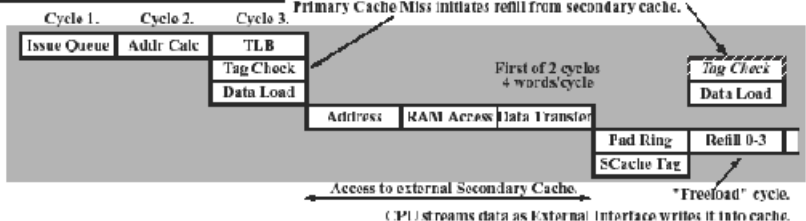
Load which hits in primary cache:



Store which hits in primary cache:

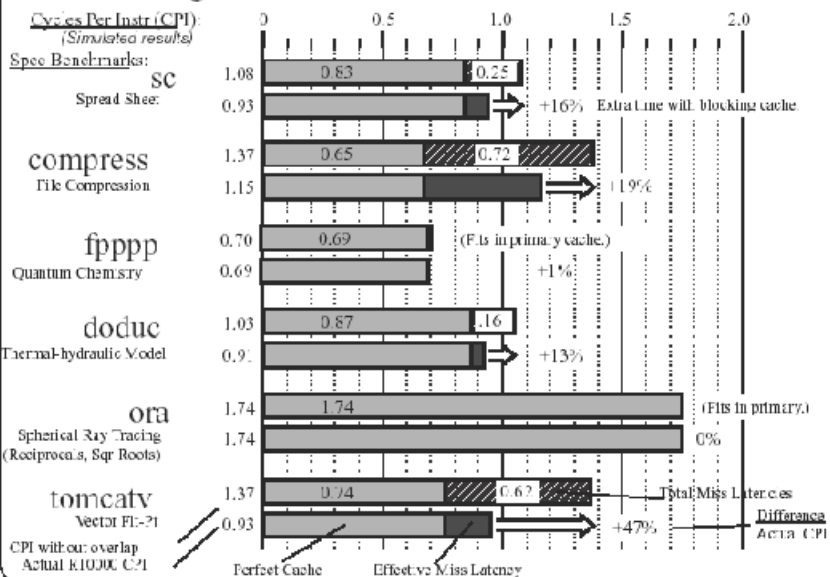


Load which misses in primary cache:

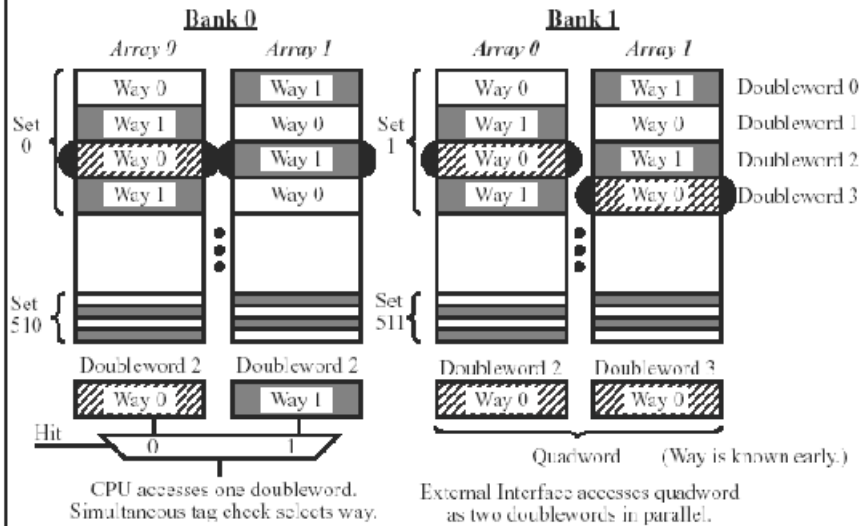


Non-blocking Cache

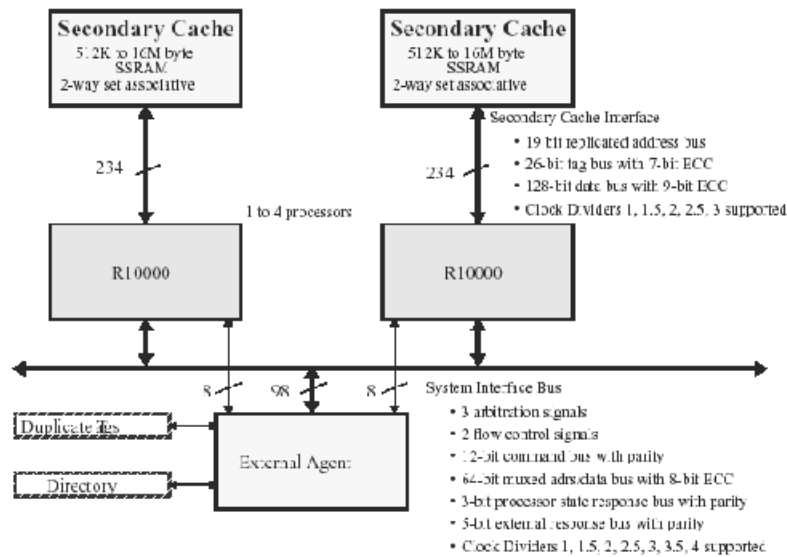
Concurrent refill times reduce effective cache latency

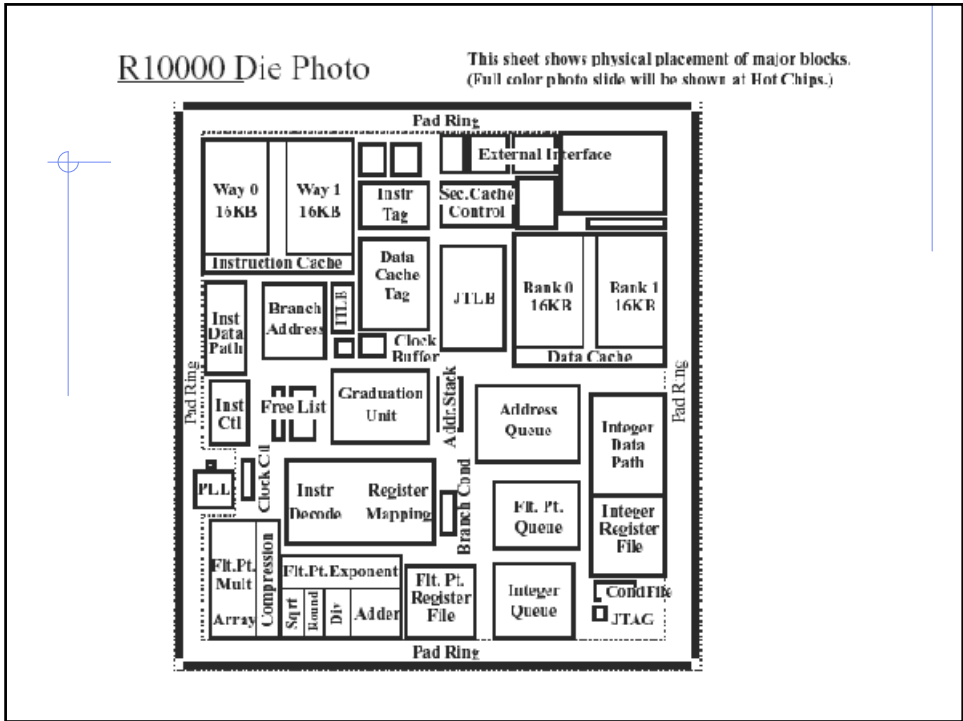
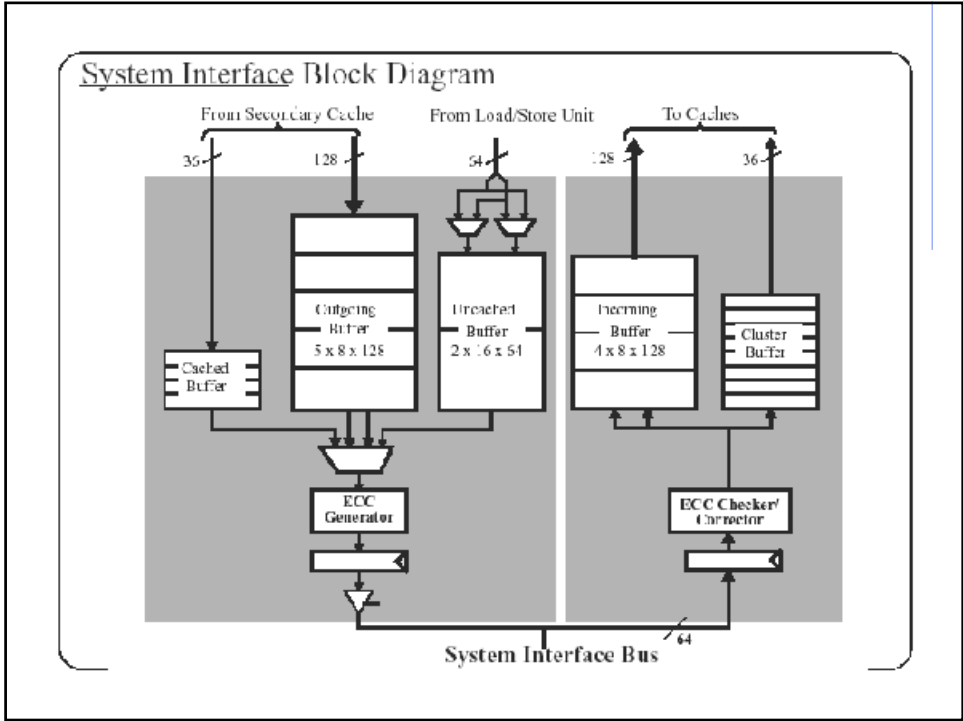


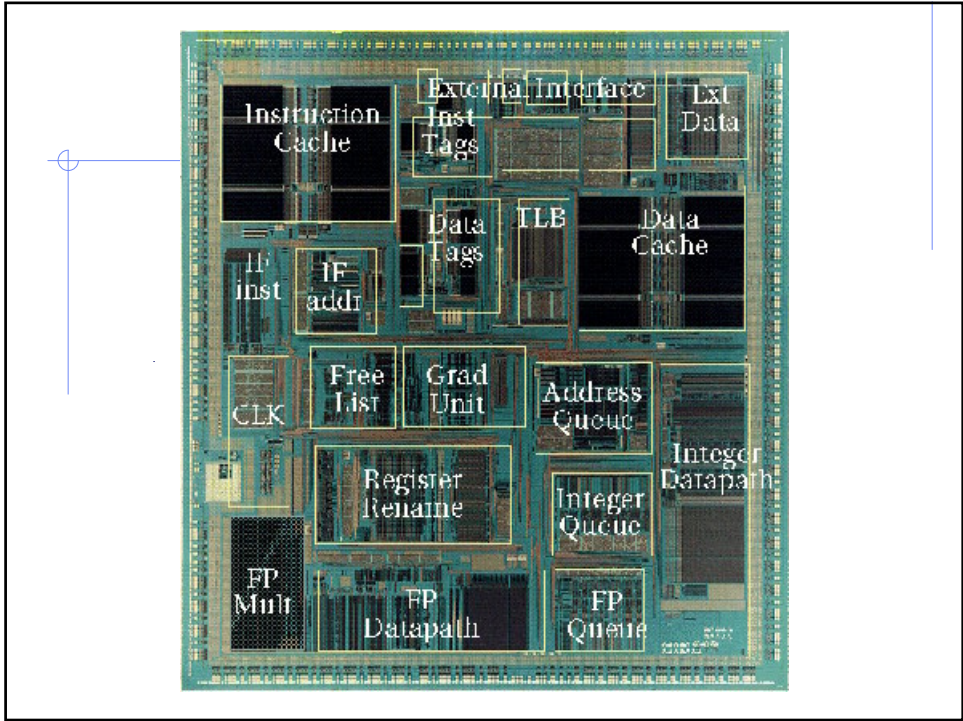
Data Cache Interleaving



System Configurations







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